Trey Boehm

contact@treyboehm.com

Education

Master of Science in Engineering ⋆ University of Texas at Austin .... December 2021

Technical focus: Architecture, Computer Systems, and Embedded Systems .... GPA: 4.00

Coursework: System-on-chip design, parallelism & locality, verification, VLSI, compilers, operating systems, data science, embedded systems, high-speed computer arithmetic, probability & stochastic processes.

Bachelor of Science in Electrical Engineering ⋆ University of Texas at Austin .... May 2020

Technical focus: Computer Architecture and Embedded Systems .... GPA: 3.92

Experience

Silicon Validation Debug Tools Engineer Apple Inc. .... January 2022 — present
 – Maintain testplans and build automated validation tests for DFD tracing IPs across all Apple SOCs.
 – Develop a Python hardware access library, accompanying IP abstractions, and processing for scan and memory dumps.
 – Support hardware and software debugs utilizing the above tools in both pre- and post-silicon environments.
 – Maintain a flexible Python-based testing framework (from the 2019 internship) for silicon IP and system validation, large-scale OS stress testing, and shmoos for process characterization.

GPU Design Verification Intern Apple Inc. .... Summer 2021
 – Expanded random shader support for additional instructions and next-generation graphics features.
 – Enabled earlier feature bringup and exposed bugs in assertions, scoreboards, and checkers.

CPU Design Verification Intern Apple Inc. .... Summer 2020
 – Wrote a stimulus generator for the external debug interface via a C++ / SystemVerilog transactor.
 – Enabled external SPR accesses on a smaller model of the core, resulting in a tenfold runtime reduction.

Operating Systems Teaching Assistant ⋆ University of Texas at Austin ...... Fall 2019, Spring 2020
 – Enabled the Pintos OS to run with any GCC and host OS by fixing compatibility issues in the linker scripts and Makefiles.
 – Wrote Bash and Expect scripts to simplify running OS test cases and automate the grading process.

Silicon Validation Debug Tools Intern Apple Inc. .... Summer 2019
 – Built a validation and stress-rack testing environment around a Python hardware interface. This was part of the larger goal to overhaul the post-silicon testing framework and unify Python convergence efforts.

Skills

 – Languages, by proficiency: Python, C, Verilog, Make, Bash, Common Lisp, Emacs Lisp, Tcl and Expect.
 – Hardware: comfortable using an oscilloscope, signal generator, and logic analyzer. I build guitar effects pedals and use an oscilloscope and signal generator to debug circuit issues. I have used logic/protocol analyzers in university for embedded systems and RTOS debug.